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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/832,913 | 04/10/2001 | A. Nicholas Sporck | P136-US | 5250 |

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| EXAMINER |
|---|
| HOLLINGTON, JERMELE M |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2829 | 8 |

DATE MAILED: 09/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application N . | Applicant(s) | |
|---|---|---|---|
| | 09/832,913 | SPORCK ET AL. | |
| | Examiner | Art Unit | |
| | Jermele M. Hollington | 2829 | |

*-- Th MAILING DATE f this communication app ars on th c ver she t with the corresp ndence address --*

**Period f r Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 April 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5&7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

The examiner will like to note to the applicants that the preliminary amendment filed on April 10, 2001 has been entered in the application. However, there are no papers of the preliminary amendment found in the application. The examiner will like to ask the applicants to send a copy of the preliminary amendment in response to this office action.

### *Drawings*

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: item 204 in Fig. 2. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, an electric circuit disposed on said daughter card [claims 2, 20 and 50], an electric circuit disposed on each of said plurality of daughter cards [claim 10], an electric circuit disposed on each of said at least three daughter cards [claim 17] and daughter means for physically supporting at least portion of an electric circuit [claim 42] must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

3. Claim 1 is objected to because of the following informalities: in line 2, "test (1)" should be --tester--. Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

5. Claims 2-7, 10-15, 17, 20-25, 38-39 and 42-57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 2, 10, 17, 20, 42 and 50, it is not clear what represents "an electric circuit." In the specification on page 9, paragraph [0017], describes what is considered to be a probe card assembly. However, the specification does not point out what is the electric circuit.

For examination purposes, the examiner assumes that "an electric circuit" is a processing circuitry. Since claims 3-7 depend off of claim 2, claims 11-15 depend off of claim 10, claims 21-25 and 38-39 depend off of claim 20, claims 43-49 depend off of claim 42 and claims 51-57 depends off of claim 50, they are also considered rejected.

### *Claim Rejections - 35 USC § 102*

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-7, 19-25, 37-39, 42, 45-50 and 55-57 are rejected under 35 U.S.C. 102(b) as being anticipated by admitted prior art of Fig. 3B.

Regarding claim 1, the admitted prior art of Fig. 3B discloses a probe card assembly (100 shown in Fig. 1A) for electrically communicating test data between a semiconductor test apparatus (120 shown in Fig. 1A) and a semiconductor device under test [not shown see page 2 lines 7-8], the probe card assembly comprising a substrate (printed circuit board 102) con figured to electrically contact the semiconductor tester apparatus (120), a plurality of probes (108) configured to electrically contact the semiconductor device under test [not shown see page 2 lines 7-8], the plurality of probes (108) located to a first side of the substrate (102) and a daughter card (mechanism 104) secured to a second side of the substrate (102) wherein the daughter card (104) being substantially coplanar to the substrate(102).

Regarding claim 2, the admitted prior art of Fig. 3B further comprising an electric circuit (processing circuitry 302) is disposed on the daughter card (104).

Regarding claim 3, the admitted prior art of Fig. 3B discloses the electric circuit (302) includes active circuit elements (traces 150b and 150c).

Regarding claim 4, the admitted prior art of Fig. 3B discloses the electric circuit (302) is configured to enhance test capabilities of the semiconductor test apparatus (120) [see page 4 paragraph [0008] lines 7-8].

Regarding claim 5, the admitted prior art of Fig. 3B discloses the electric circuit (302) is configured to customize at least portion of the test data to test needs of said semiconductor device under test (not shown) [see page 4 paragraph [0008] lines 7-8].

Regarding claim 6, the admitted prior art of Fig. 3B discloses the test data comprises test signals generated by said semiconductor test apparatus (120) and the electric circuit (302) customizes at least portion of the test signals [see page 4 paragraph [0008] lines 4-13].

Regarding claim 7, the admitted prior art of Fig. 3B discloses the test data comprises response signals generated by said semiconductor device under test (not shown) and the electric circuit (302) customizes at least portion of the response signals [see page 4 paragraph [0008] lines 4-13].

Regarding claim 19, the admitted prior art of Fig. 3B discloses a method of making a probe card assembly (100 shown in Fig. 1A), the method comprising providing a substrate (printed circuit board 102) including a plurality of tester contacts (130), securing a plurality of probes (108) to a first side of the substrate (102) and configured to electrically contact a semiconductor device under test [not shown see page 2 lines 7-8], and securing a daughter card (mechanism 104) to a second side of the substrate (102) wherein the daughter card (104) being substantially coplanar to the substrate(102).

Regarding claim 20, the admitted prior art of Fig. 3B further comprising providing an electric circuit (processing circuitry 302) and disposing the electric circuit (302) on the daughter card (104).

Regarding claim 21, the admitted prior art of Fig. 3B discloses the electric circuit (302) includes active circuit elements (traces 150b and 150c).

Regarding claim 22, the admitted prior art of Fig. 3B discloses the electric circuit (302) is configured to enhance test capabilities of the semiconductor test apparatus (120) [see page 4 paragraph [0008] lines 7-8].

Regarding claim 23, the admitted prior art of Fig. 3B discloses the electric circuit (302) is configured to customize test data to test needs of said semiconductor device under test (not shown) [see page 4 paragraph [0008] lines 7-8].

Regarding claim 24, the admitted prior art of Fig. 3B discloses the test data comprises test signals to be input into the semiconductor device under test (not shown) and the electric circuit (302) customizes at least portion of the test signals [see page 4 paragraph [0008] lines 4-13].

Regarding claim 25, the admitted prior art of Fig. 3B discloses the test data comprises response signals generated by said semiconductor device under test (not shown) and the electric circuit (302) customizes at least portion of the response signals [see page 4 paragraph [0008] lines 4-13].

Regarding claims 37-39, the admitted prior art of Fig. 3B discloses the probe card assembly (100) made using the process of claims 19-20 and 22.

[Note: "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)]

Regarding claim 42, the admitted prior art of Fig. 3B discloses a probe card assembly (100 shown in Fig. 1A) comprising a printed circuit means (102) for electrically communicating with a semiconductor tester apparatus (120), contact means (probes 108) configured to

electrically communicating with semiconductor device under test [not shown see page 2 lines 7-8], the contact means (108) being secured to a first side of the printed circuit means (102) and daughter card means (mechanism 104) for physically supporting at least portion of an electric circuit (processing circuitry 302), the daughter card means (104) secured to a second side of the printed circuit means (102) wherein the daughter card (104) being substantially coplanar to the printed circuit means (102).

Regarding claim 45, the admitted prior art of Fig. 3B discloses the electric circuit (302) includes processing means [processing circuitry] for processing test data for testing the semiconductor device under test (not shown).

Regarding claim 46, the admitted prior art of Fig. 3B discloses the processing means (302) enhances test capabilities of the semiconductor test apparatus (120) [see page 4 paragraph [0008] lines 7-8].

Regarding claim 47, the admitted prior art of Fig. 3B discloses the processing means (302) customizes the test data to meet test needs of said semiconductor device under test (not shown) [see page 4 paragraph [0008] lines 7-8].

Regarding claim 48, the admitted prior art of Fig. 3B discloses the test data comprises test signals to be input into the semiconductor device under test (not shown) and the processing means (302) customizes at least portion of the test signals [see page 4 paragraph [0008] lines 4-13].

Regarding claim 49, the admitted prior art of Fig. 3B discloses the test data comprises response signals generated by said semiconductor device under test (not shown) and the

processing means (302) customizes at least portion of the response signals [see page 4 paragraph [0008] lines 4-13].

Regarding claim 50, the admitted prior art of Fig. 3B discloses a probe card assembly (100 shown in Fig. 1A) for electrically communicating test data between a semiconductor test apparatus (120 shown in Fig. 1A) and a semiconductor device under test [not shown see page 2 lines 7-8], the probe card assembly comprising a printed circuit board (102) con figured to electrically contact the semiconductor tester apparatus (120), a plurality of probes (108) configured to electrically contact the semiconductor device under test [not shown see page 2 lines 7-8], the plurality of probes (108) located to a first side of the substrate (102), a daughter card (mechanism 104) secured to the printed circuit board (102) wherein the daughter card (104) being substantially coplanar to the printed circuit board (102) and an electric circuit (processing circuitry 302) enhances test capabilities of the semiconductor test apparatus (120) [see page 4 paragraph [0008] lines 7-8] and is disposed on the daughter card (104).

Regarding claim 55, the admitted prior art of Fig. 3B discloses the electric circuit (302) enhances test capabilities of the semiconductor test apparatus (120) by processing at least portion of the test data.

Regarding claim 56, the admitted prior art of Fig. 3B discloses the test data comprises test signals generated by the semiconductor tester apparatus (120) and the electric circuit (302) processes at least portion of the test signals [see page 4 paragraph [0008] lines 4-13].

Regarding claim 57, the admitted prior art of Fig. 3B discloses the test data comprises response signals generated by said semiconductor device under test (not shown) and the electric

circuit (302) processes at least portion of the response signals [see page 4 paragraph [0008] lines 4-13].

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 8-18, 26-36, 40-41, 43-44 and 51-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art of Fig. 3B.

Regarding claims 8-9, 16, 18, 26-27, 34, 36, and 51-55 the admitted prior art of Fig. 3B discloses the claimed invention except for a plurality of daughter cards. It would have been an obvious matter of design choice to have a plurality of daughter cards, since such a modification would have involved a mere duplication of parts of a component. A duplication of parts is generally recognized as being within the level of ordinary skill in the art. *In re Harza*, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

Regarding claims 10, 17, 28, 35, the admitted prior art of Fig. 3B further comprising an electric circuit (processing circuitry 302) is disposed on the plurality of daughter cards (104).

Regarding claims 11, 29, the admitted prior art of Fig. 3B discloses the electric circuit (302) includes active circuit elements (traces 150b and 150c).

Regarding claims 12, 30, the admitted prior art of Fig. 3B discloses the electric circuit (302) is configured to enhance test capabilities of the semiconductor test apparatus (120) [see page 4 paragraph [0008] lines 7-8].

Regarding claims 13, 31, the admitted prior art of Fig. 3B discloses the electric circuit (302) is configured to customize at least portion of the test data to test needs of said semiconductor device under test (not shown) [see page 4 paragraph [0008] lines 7-8].

Regarding claims 14, 32, the admitted prior art of Fig. 3B discloses the test data comprises test signals generated by said semiconductor test apparatus (120) and the electric circuit (302) customizes at least portion of the test signals [see page 4 paragraph [0008] lines 4-13].

Regarding claims 15, 33, the admitted prior art of Fig. 3B discloses the test data comprises response signals generated by said semiconductor device under test (not shown) and the electric circuit (302) customizes at least portion of the response signals [see page 4 paragraph [0008] lines 4-13].

Regarding claims 40-41, the admitted prior art of Fig. 3B discloses the probe card assembly (100) made using the process of claims 26 and 30.

[Note: "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a

product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)]

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (703) 305-1653. The examiner can normally be reached on M-F (9:00-3:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (703) 308-1680. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
September 20, 2002

9/24/02

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800